

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74HC573AP, TC74HC573AF

### Octal D-Type Latch with 3-State Output

The TC74HC573A is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Its 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ).

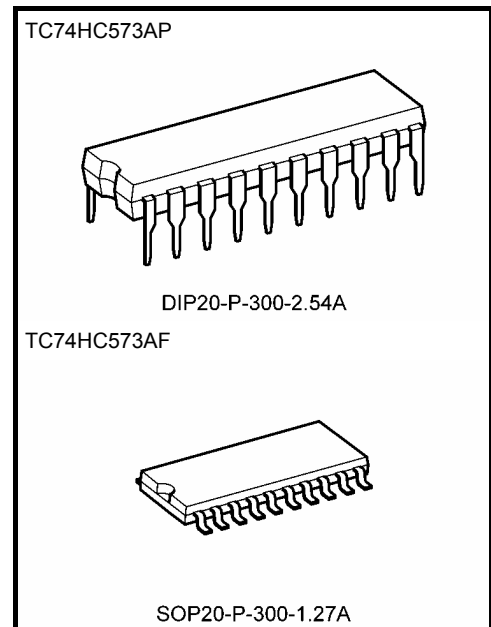
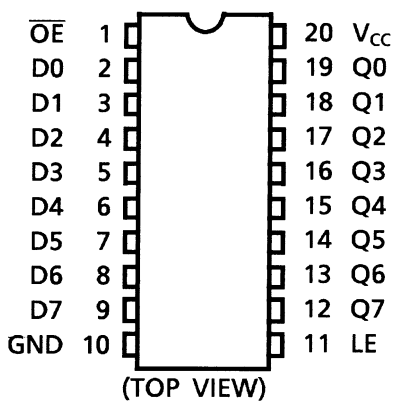
When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $t_{pd} = 13 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 6 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS573

### Pin Assignment

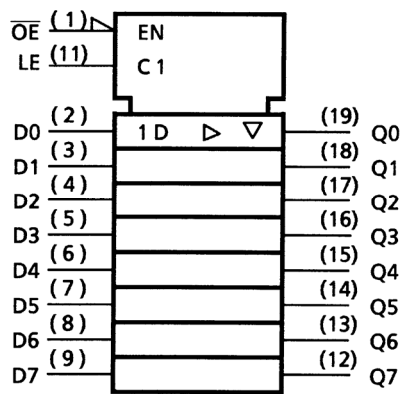


Weight

DIP20-P-300-2.54A : 1.30 g (typ.)

SOP20-P-300-1.27A : 0.22 g (typ.)

IEC Logic Symbol



Truth Table

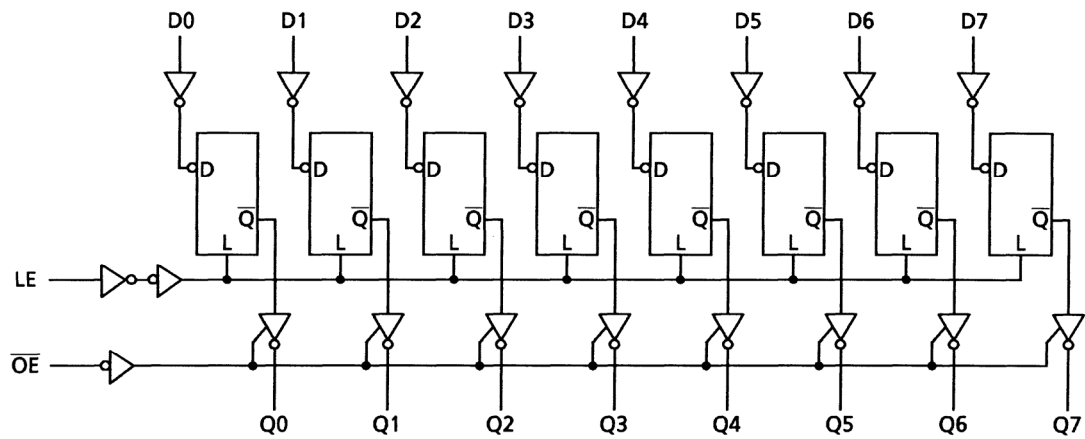
Inputs			Output
$\overline{OE}$	$LE$	$D$	$Q$
H	X	X	HZ
L	L	X	$Q_n$
L	H	L	L
L	H	H	H

X: Don't care

HZ: High impedance

$Q_n$ : Q outputs are latched at the time when the  $LE$  input is taken to a low logic level.

System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^\circ\text{C}$ . From  $T_a = 65$  to  $85^\circ\text{C}$  a derating factor of  $-10$  mW/°C shall be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

## DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit		
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V <sub>IH</sub>	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V		
Low-level input voltage	V <sub>IL</sub>	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	V		
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V	
				4.5	4.4	4.5	—	4.4	—		
				6.0	5.9	6.0	—	5.9	—		
			I <sub>OH</sub> = -6 mA		4.5	4.18	4.31	—	4.13		—
I <sub>OH</sub> = -7.8 mA		6.0	5.68	5.80	—	5.63	—				
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V	
				4.5	—	0.0	0.1	—	0.1		
				6.0	—	0.0	0.1	—	0.1		
			I <sub>OL</sub> = 6 mA		4.5	—	0.17	0.26	—		0.33
			I <sub>OL</sub> = 7.8 mA		6.0	—	0.18	0.26	—		0.33
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.5	—	±5.0	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	4.0	—	40.0	μA	

Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
				V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (LE)	t <sub>W</sub> (H)	—	—	2.0	—	75	ns
				4.5	—	15	
				6.0	—	13	
Minimum set-up time (data)	t <sub>s</sub>	—	—	2.0	—	50	ns
				4.5	—	10	
				6.0	—	9	
Minimum hold time (data)	t <sub>h</sub>	—	—	2.0	—	5	ns
				4.5	—	5	
				6.0	—	5	

## AC Characteristics (input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			CL (pF)	V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$ $t_{THL}$	—	50	2.0	—	20	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation delay time (LE-Q)	$t_{pLH}$ $t_{pHL}$	—	50	2.0	—	50	115	—	145	ns
				4.5	—	15	23	—	29	
				6.0	—	13	20	—	25	
			150	2.0	—	60	155	—	195	
				4.5	—	20	31	—	39	
				6.0	—	17	26	—	33	
Propagation delay time (D-Q)	$t_{pLH}$ $t_{pHL}$	—	50	2.0	—	42	110	—	140	ns
				4.5	—	14	22	—	28	
				6.0	—	12	19	—	24	
			150	2.0	—	57	150	—	190	
				4.5	—	19	30	—	38	
				6.0	—	16	26	—	32	
Output enable time	$t_{pZL}$ $t_{pZH}$	$R_L = 1 \text{ k}\Omega$	50	2.0	—	55	140	—	175	ns
				4.5	—	17	28	—	35	
				6.0	—	14	24	—	30	
			150	2.0	—	66	180	—	225	
				4.5	—	22	36	—	45	
				6.0	—	19	31	—	38	
Output disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1 \text{ k}\Omega$	50	2.0	—	40	125	—	155	ns
				4.5	—	17	25	—	31	
				6.0	—	15	21	—	26	
Input capacitance	$C_{IN}$	—	—	—	—	5	10	—	10	pF
Output capacitance	$C_{OUT}$	—	—	—	—	10	—	—	—	pF
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	—	—	51	—	—	—	pF

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

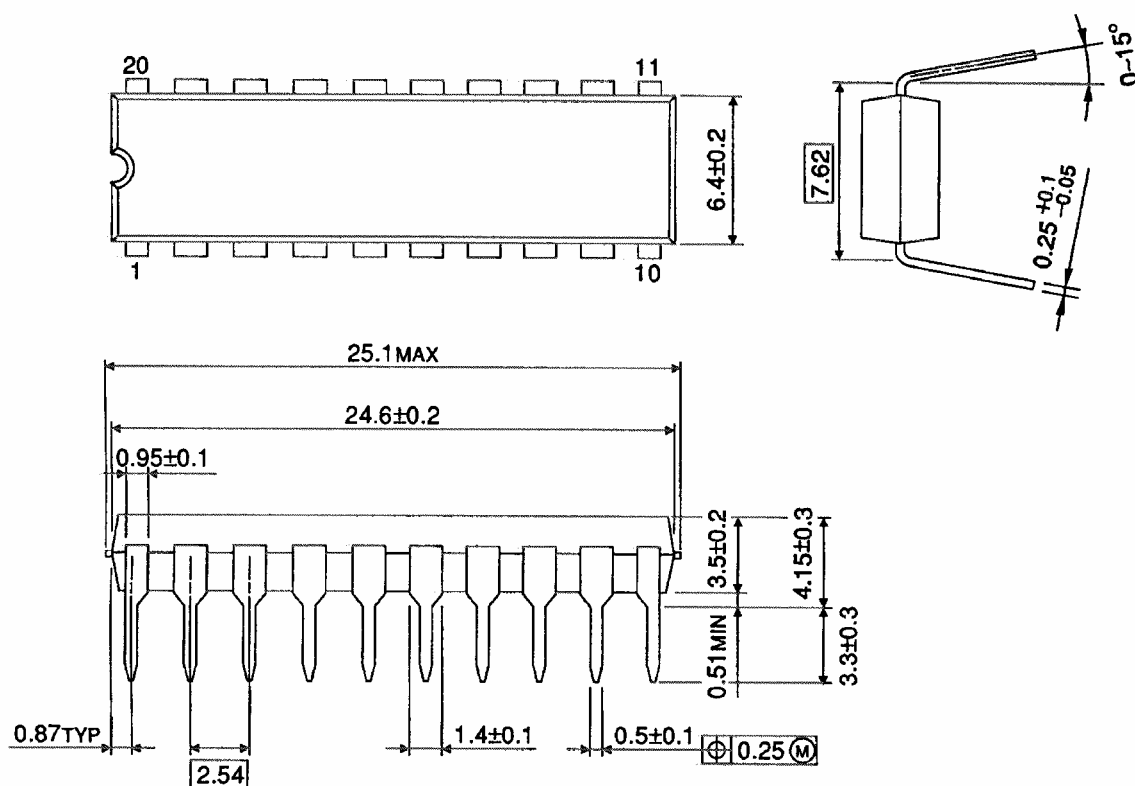
And the total  $C_{PD}$  when n pcs. of latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 33 + 18 \cdot n$$

## Package Dimensions

DIP20-P-300-2.54A

Unit : mm

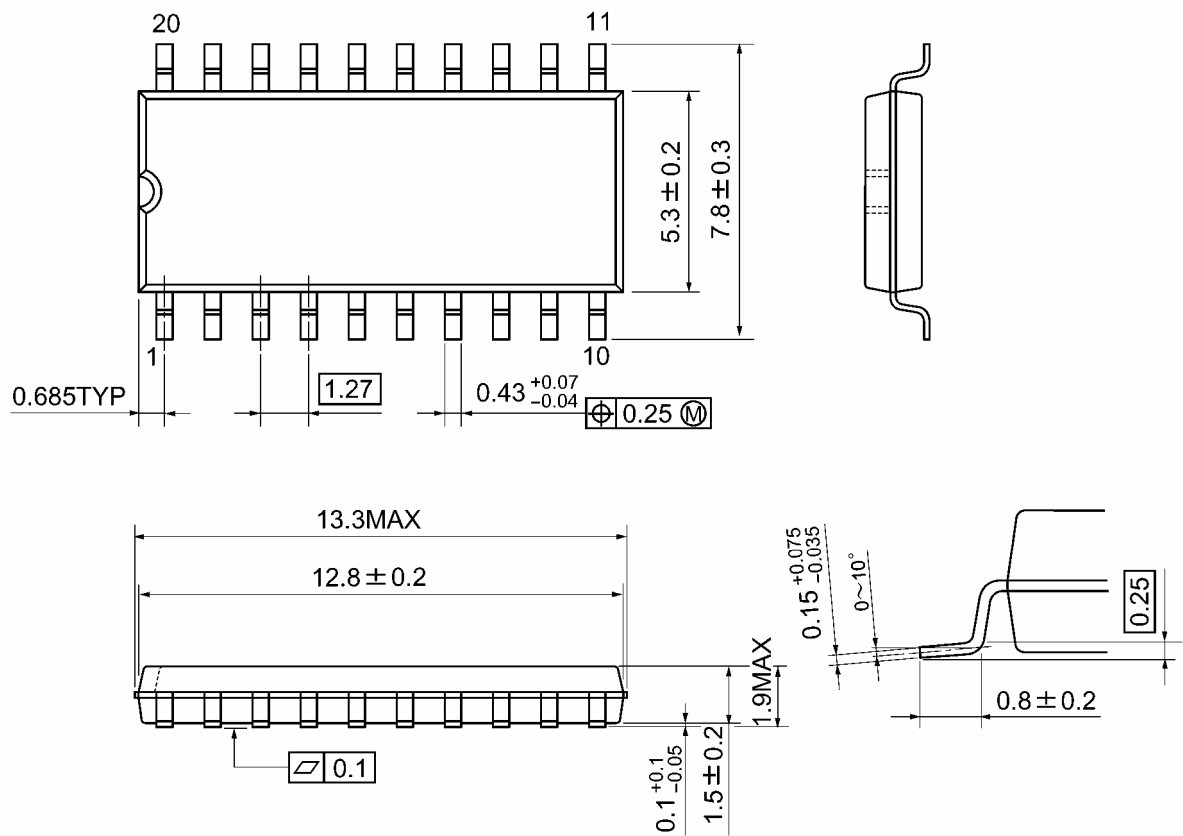


Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A

Unit: mm



Weight: 0.22 g (typ.)

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